What is claimed is:

1. A circuit comprising:

a discrete-time FIR (Finite Impulse Response) filter comprising n multiplier units to implement a filter response $[\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$, where t is a time index;

a data generator to provide a discrete-time sequence of desired voltages $d(t)$, $t = 1,2,\ldots,T$,

a multiplier to provide a sequence of voltages $Kd(t)$, $t = 1,2,\ldots,T$, where K is a scalar;

a filter increment generator to provide, for $t = 1,2,\ldots,T$, n voltages indicative of n filter increments $[\delta\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$;

at least one summer to perform the sum $[\bar{h}(t)]_i + \delta\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$ to update the filter response;

an overflow counter to provide an overflow count indicative of the number of numerical overflows in the at least one summer during the time period $t = 1,2,\ldots,T$;

wherein the scalar K is increased by a first increment if after completion of the time period $t = 1,2,\ldots,T$ the overflow count and a threshold satisfy a first relationship.

2. The circuit as set forth in claim 1, wherein the scalar K is decreased by a second increment if after completion of the time period $t = 1,2,\ldots,T$ the overflow count and the threshold satisfy a second relationship.

3. The circuit as set forth in claim 2, wherein the first increment is equal to the second increment.

4. The circuit as set forth in claim 3, wherein

the overflow count and the threshold satisfy the first relationship if and only if the overflow count is greater than the threshold;

the overflow count and the threshold satisfy the second relationship if and only if the overflow count is less than or equal to the threshold; and

the first increment is positive.

5. The circuit as set forth in claim 1, wherein

the overflow count and the threshold satisfy the first relationship if and only if the overflow count is greater than the threshold; and

the first increment is positive.

6. The circuit as set forth in claim 5, the multiplier comprising:

a voltage-to-current converter to provide as output a current I_{VC} indicative of the voltage $d(t)$; and

a current steering digital-to-analog converter to shunt a portion of I_{VC} to provide as output at time t a current indicative of $Kd(t)$.

7. The circuit as set forth in claim 2, wherein

the overflow count and the threshold satisfy the first relationship if and only if the overflow count is greater than the threshold;

the overflow count and the threshold satisfy the second relationship if and only if the overflow count is less than or equal to the threshold; and

the first increment and the second increment are positive.

8. The circuit as set forth in claim 1, wherein the voltage $d(t)$ is a differential voltage.

9. A computer system comprising:

a board comprising a fist transmission line an a second transmission line; and

a receiver coupled to the first an second transmission lines, the receiver comprising:

a discrete-time FIR (Finite Impulse Response) filter comprising n multiplier units to implement a filter response $[\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$, where t is a time index;

a data generator to provide a discrete-time sequence of desired voltages $d(t), t = 1,2,\ldots,T$,

a multiplier to provide a sequence of voltages $Kd(t), t = 1,2,\ldots,T$, where K is a scalar;

a filter increment generator to provide, for $t = 1,2,\ldots,T$, n voltages indicative of n filter increments $[\delta\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$;

at least one summer to perform the sum $[\bar{h}(t)]_i + \delta\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$ to update the filter response;

an overflow counter to provide an overflow count indicative of the number of numerical overflows in the at least one summer during the time period $t = 1,2,\ldots,T$;

wherein the scalar K is increased by a first increment if after completion of the time period $t = 1,2,\ldots,T$ the overflow count and a threshold satisfy a first relationship.

10. The computer system as set forth in claim 9, wherein the scalar K is decreased by a second increment if after completion of the time period $t = 1,2,\ldots,T$ the overflow count and the threshold satisfy a second relationship.

11. The computer system as set forth in claim 9, wherein the voltage $d(t)$ is a differential voltage.

12. A method to calibrate a scale factor in an adaptive equalizer, the scale factor being used to multiply a sequence of desired voltages used in updating the equalizer during a training sequence, the method comprising:

updating the adaptive equalizer over the training sequence;

counting the number of numerical overflows occurring while updating the adaptive equalizer over the training sequence;

increasing the scale factor by a first increment if the number of numerical overflows and a threshold satisfy a first relationship.

13. The method as set forth in claim 12, wherein the scalar is decreased by a second increment if the number of numerical overflows and the threshold satisfy a second relationship.

14. The circuit as set forth in claim 13, wherein the first increment is equal to the second increment.

15. The circuit as set forth in claim 14, wherein

the overflow count and the threshold satisfy the first relationship if and only if the overflow count is greater than the threshold;

the overflow count and the threshold satisfy the second relationship if and only if the overflow count is less than or equal to the threshold; and

the first increment is positive.

16. The circuit as set forth in claim 12, wherein

the overflow count and the threshold satisfy the first relationship if and only if the overflow count is greater than the threshold; and

the first increment is positive.

17. The circuit as set forth in claim 13, wherein

the overflow count and the threshold satisfy the first relationship if and only if the overflow count is greater than the threshold;

the overflow count and the threshold satisfy the second relationship if and only if the overflow count is less than or equal to the threshold; and

the first increment and the second increment are positive.

18. The circuit as set forth in claim 12, wherein the sequence of desired voltages are differential voltages.